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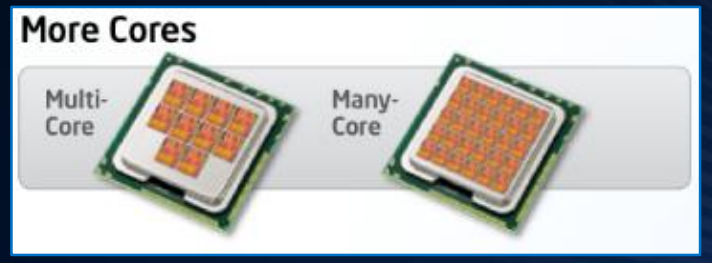
КАК INTEL® ADVISOR ПОМОЖЕТ ИСПОЛЬЗОВАТЬ ПЛАТФОРМЫ INTEL® НА 100%

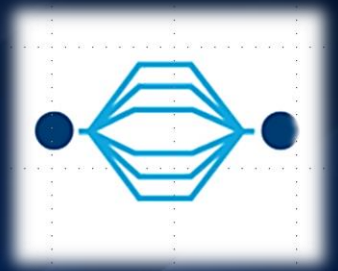
Andrey Golovin, 29-Oct-2019, Moscow

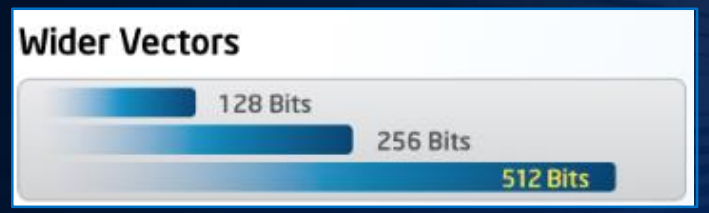
INTEL ADVISOR: INSIGHTS FOR ACCELERATION

Part of Intel Parallel Studio. Responses to the hardware **challenges**:

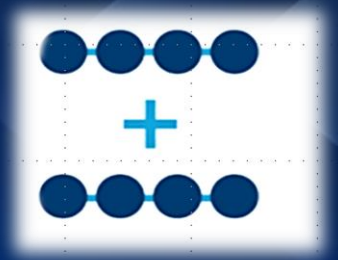


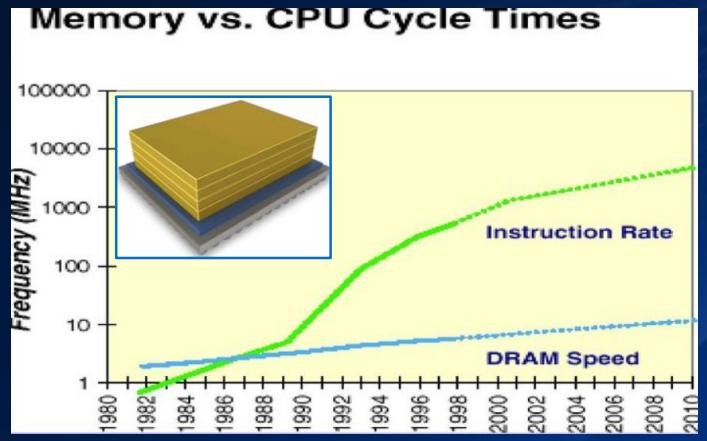
Intel multi-core ❯ Threading Workflow



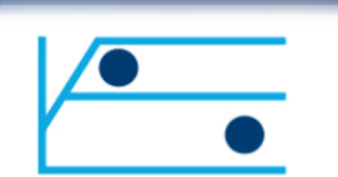


Intel SIMD AVX512 enabling ❯ Vector Workflow





Memory hierarchies complexity ❯ Roofline Workflow

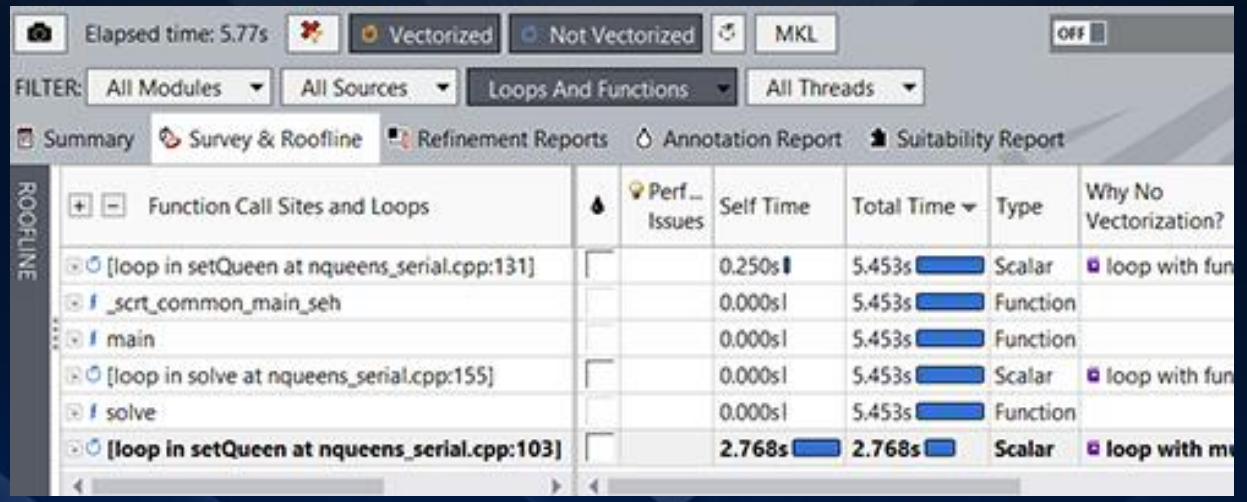


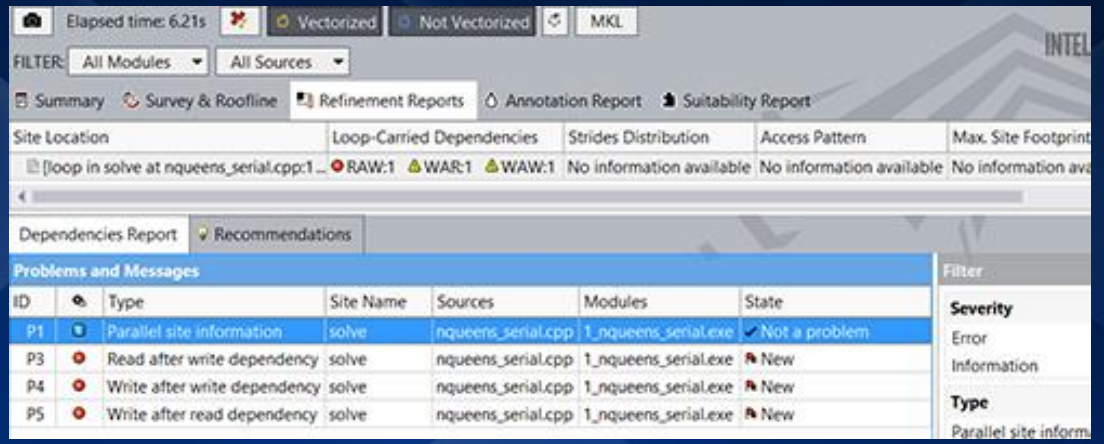
More acceleration is coming…

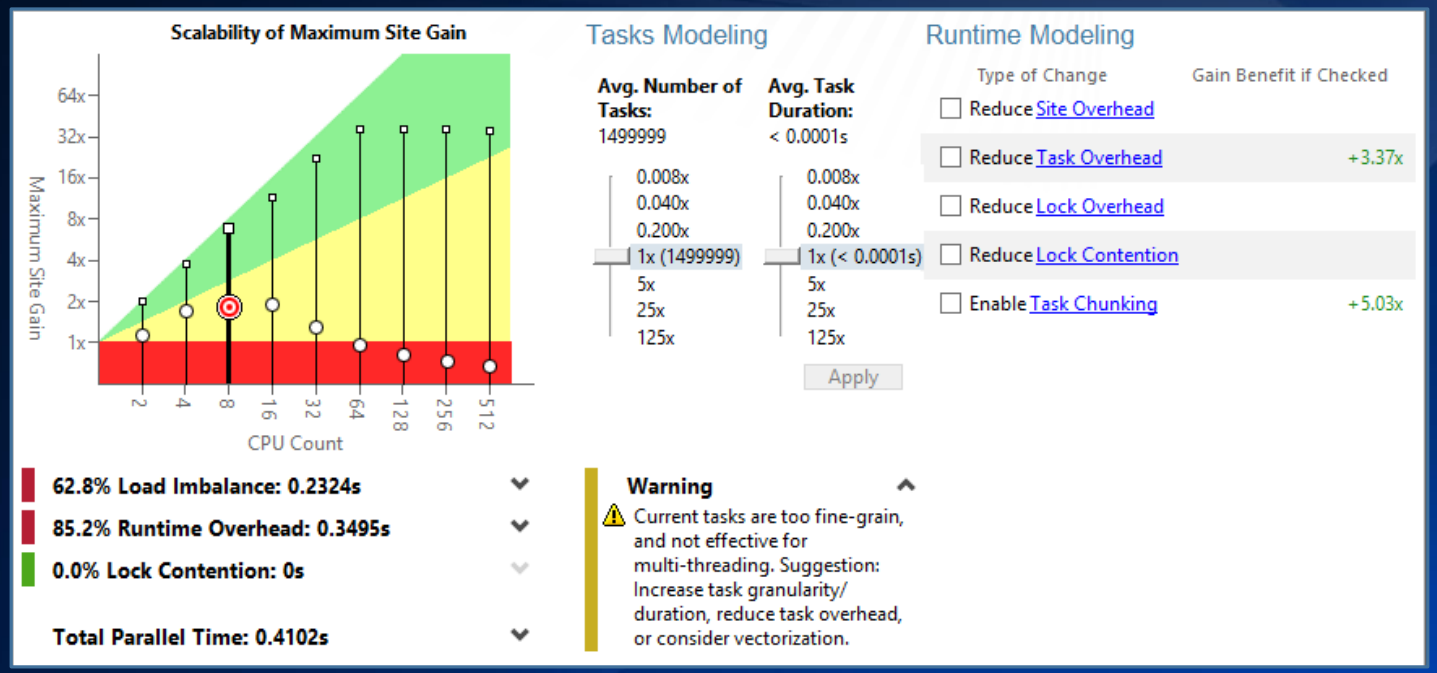
INTEL ADVISOR : THREADING WORKFLOW

Threading Advisor – multi-core performance and correctness design

- Scalability, task scheduler and imbalance modeling
- Data Dependencies “what-if” analysis





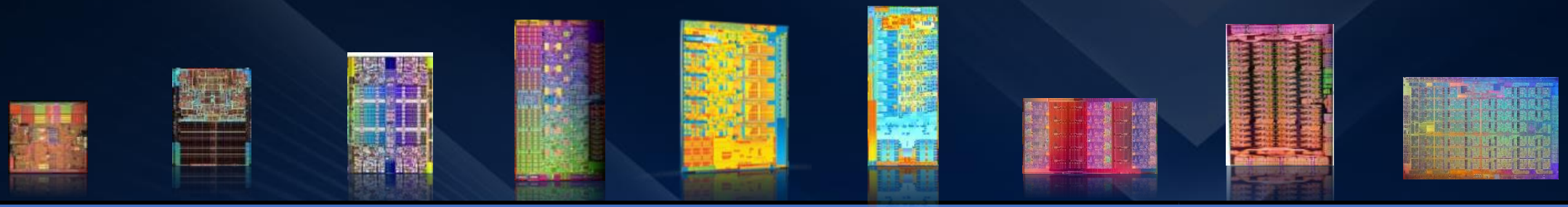


Sample Annotations

```
// Locking
ANNOTATE_LOCK_ACQUIRE();
  Body();
ANNOTATE_LOCK_RELEASE():
```

```
// Do-All Counted loops, one task
ANNOTATE_SITE_BEGIN(site);
  For (I = 0; I < N; ++) {
    ANNOTATE_ITERATION_TASK(task);
      {statement;}
  }
```

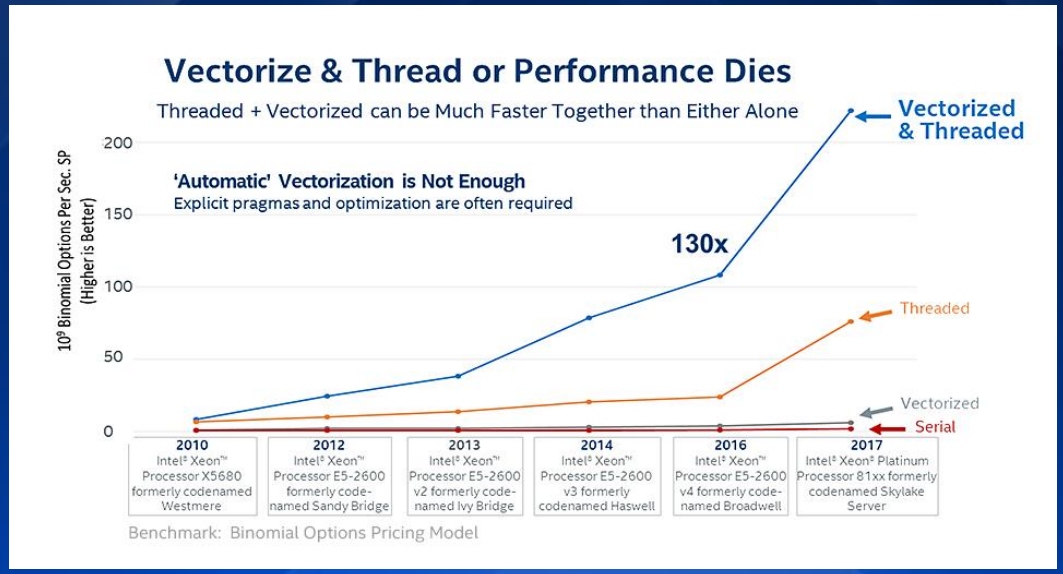
INTEL ADVISOR : VECTORIZATION WORKFLOW



	Intel® Xeon® processor 64-bit	Intel® Xeon® processor 5100 series	Intel® Xeon® processor 5500 series	Intel® Xeon® processor 5600 series	Intel® Xeon® processor code-named Sandy Bridge EP	Intel® Xeon® processor code-named Ivy Bridge EP	Intel® Xeon® processor code-named Skylake EP	Intel® Xeon Phi™ coprocessor Knights Corner	Intel® Xeon Phi™ processor & coprocessor Knights Landing[1]
SIMD Width	128	128	128	128	256	256	256	512	512

THREADING + VECTORIZATION

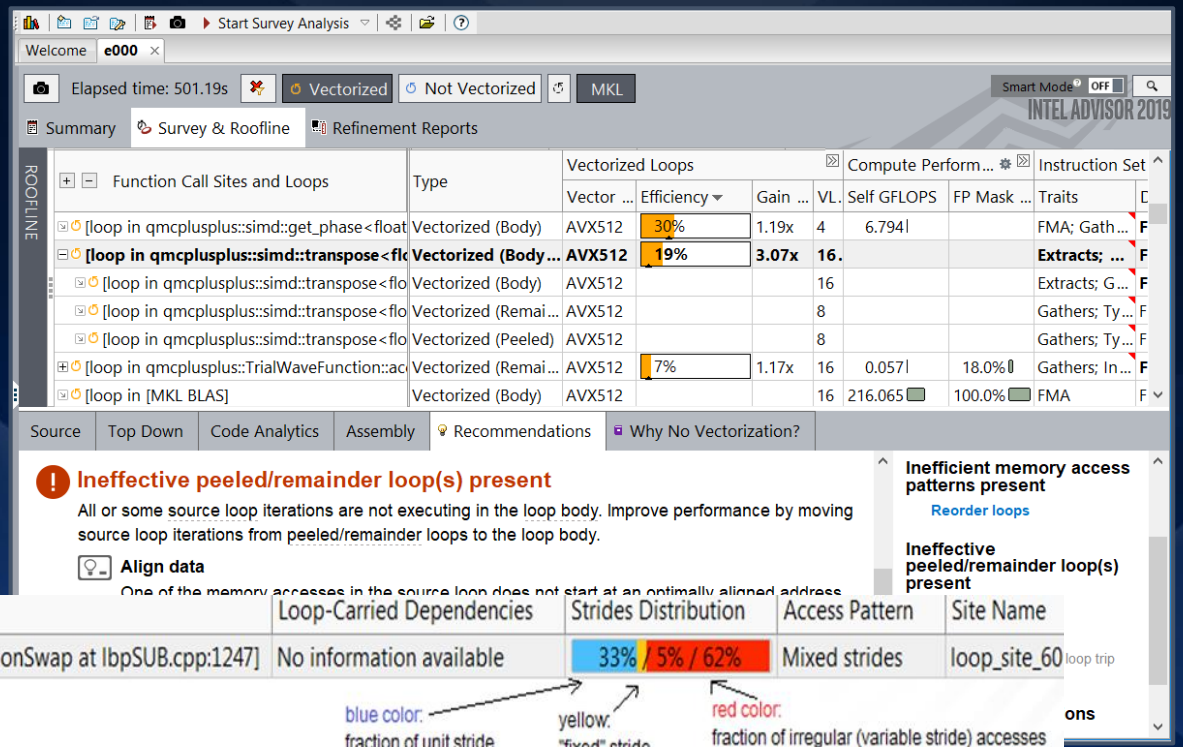
UP TO 130X FASTER ON BENCHMARK

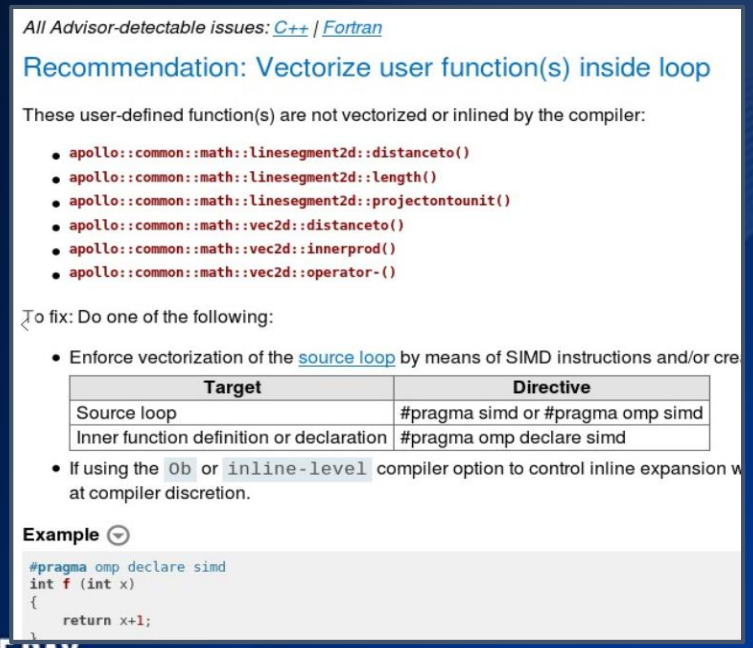


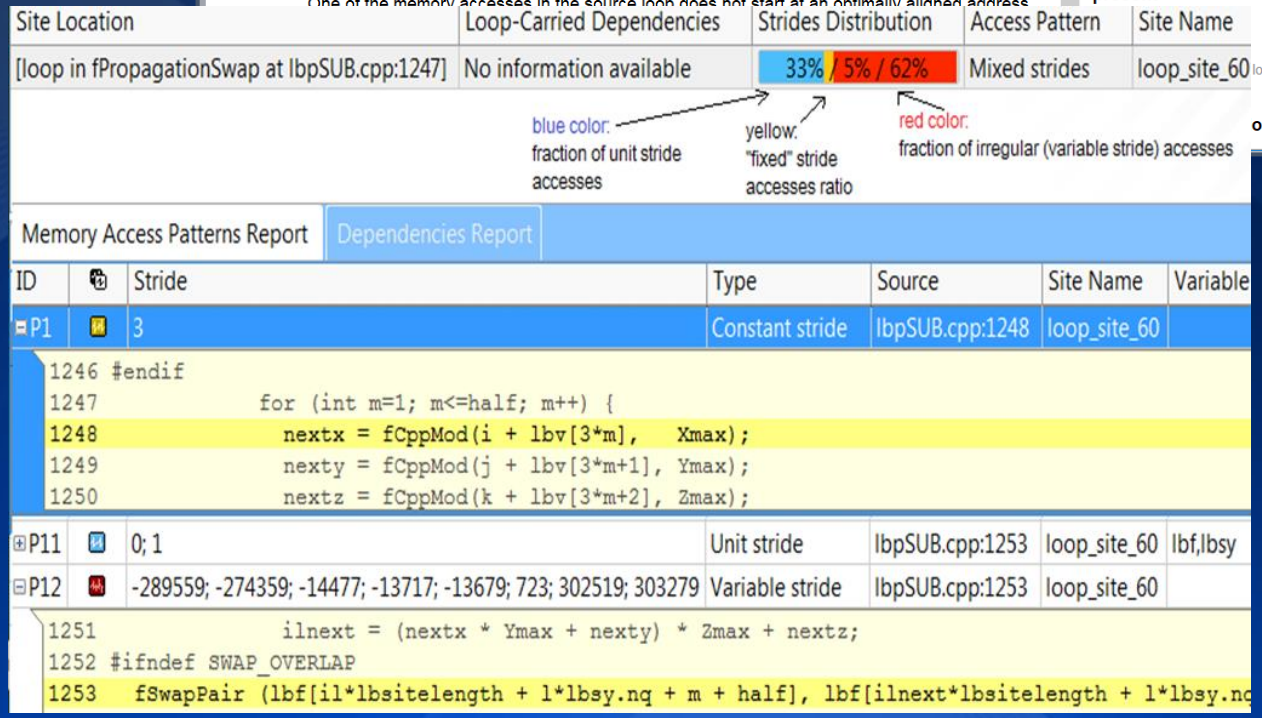
INTEL ADVISOR : VECTORIZATION WORKFLOW

Vectorization Advisor – AVX* SIMD analysis tool

- Integration with Intel Compiler perf model, SIMD / Mask register profiling
- Explicit programming model advise: “how do I fix it?”

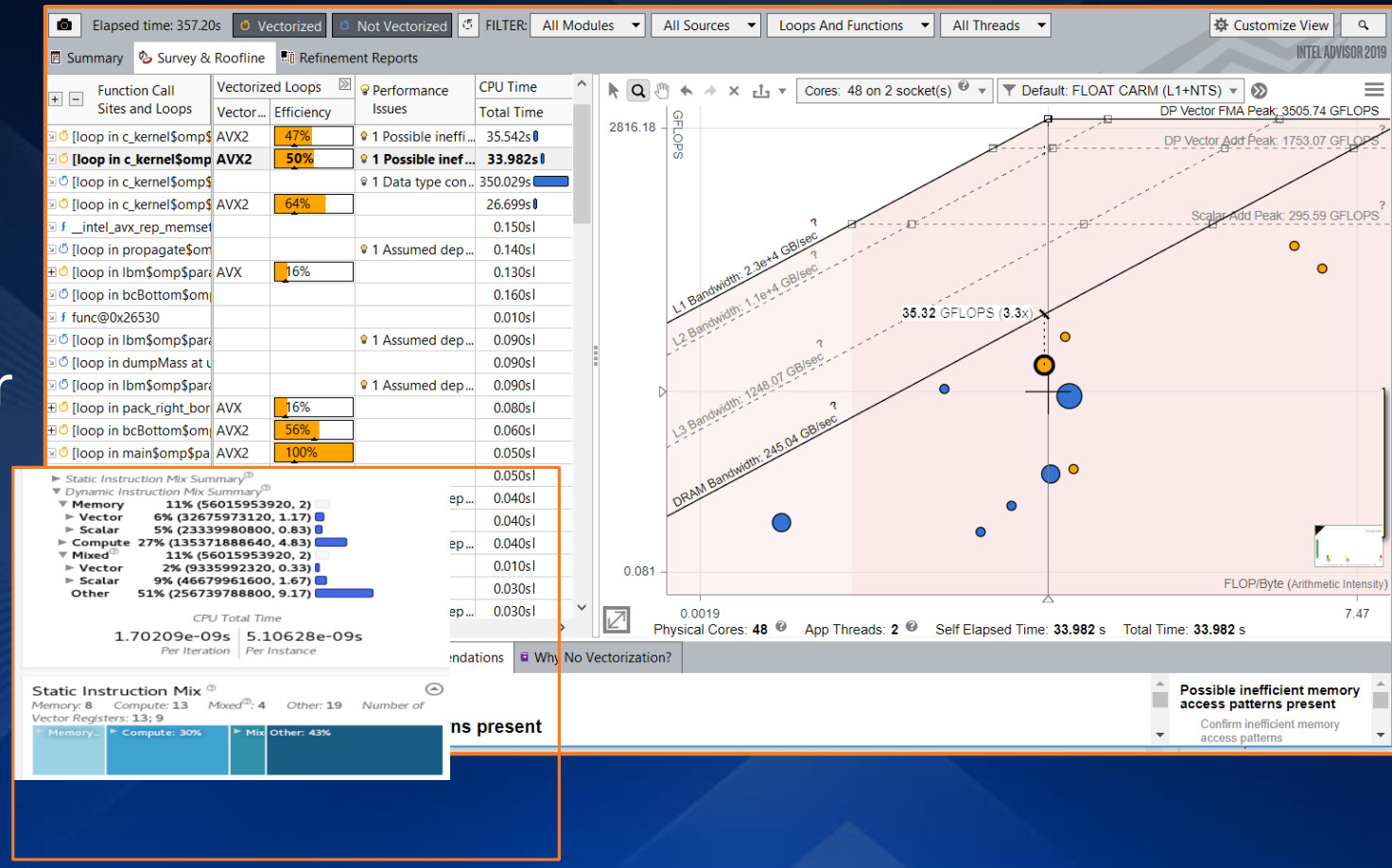






INTEL ADVISOR : ROOFLINE AND MEMORY WORKFLOW

- Deep memory hierarchies characterization and simulation
- Visually intuitive modeling
- Highlights poor performing loops
- Shows performance ‘headroom’ for each loop
- Shows likely causes of bottlenecks
- Suggests next optimization steps



Roofline model proposed by Berkeley Lab, by Williams, Waterman, Patterson:
http://www.eecs.berkeley.edu/~waterman/papers/roofline.pdf
Cache-aware Roofline model: Upgrading the loft”
(Ilic, Pratas, Sousa, INESC-ID/IST, Thec Uni of Lisbon)
http://www.inesc-id.pt/ficheiros/publicacoes/9068.pdf

INTEL ADVISOR : CUSTOMER STORIES

INTEL ADVISOR : KEY SPECIFICATIONS

Processors
- IA-32 or Intel® 64 architectures
- SSE2 or later SIMD instruction sets: Intel® Advanced Vector Extensions, Intel® Advanced Vector Extensions 2, Intel® Advanced Vector Extensions 512, and more

Operating Systems
- Windows
- Linux
- macOS (viewer only, no data collection)

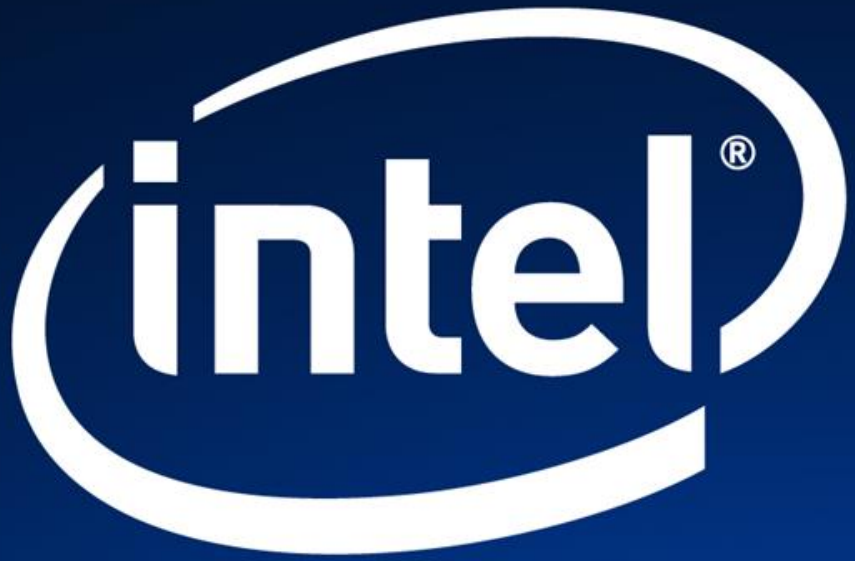
Programming Languages
- C
- C++
- Fortran

Compilers
- Compilers from Intel
- Microsoft Visual C++* compiler
- GNU Compiler Collection (GCC)*
- Other compilers that follow the same standards

Development Environments and Interfaces
- Run as stand-alone applications
- Integrated with Microsoft Visual Studio*
- Command Line interface
- Python API

https://software.intel.com/en-us/advisor

Intel Advisor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